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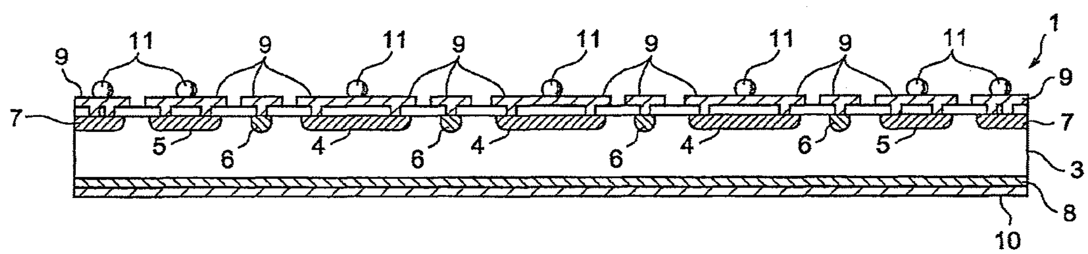
(54) SEMICONDUCTOR ENERGY DETECTOR

(57) A photodiode array 1 includes P^+ diffusion layers 4 and 5, N^+ channel stop layers 6 and 7, an N^+ diffusion layer 8 and the like. The P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7 are provided on a surface side opposite to an incident surface of a semiconductor substrate 3. The N^+ channel stop layer 6 is provided between the P^+ diffusion layers 4, 5 adjacent to each other, and exhibits a form of lattice so as to separate the P^+ diffusion layers 4, 5. The N^+ channel stop layer 7 is provided in the form of frame on the outside of an array of the P^+ diffusion layer 5 continuously with the N^+ channel stop layer 6. The N^+ channel stop layer 7 is set wider than the N^+ channel stop layer 6. To the incident surface of the semiconductor substrate 3, a scintillator is optically connected.

Fig.3



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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor energy detector for detecting an energy ray such as radiation.

BACKGROUND ART

[0002] As this type of the semiconductor energy detector, for example, one as disclosed in Japanese Patent Laid-Open Publication H5-150049 (published in 1993) has been known. This semiconductor energy detector disclosed in Japanese Patent Laid-Open Publication H5-150049 includes an N-type silicon wafer. A large number of grooves are formed on a surface of this silicon wafer, and a P-type diffusion layer is formed so as to be located on a bottom portion of each groove. Then, an electrode composed of metal such as aluminum is formed on the surface side of the silicon wafer, and is electrically connected to a part of the P-type diffusion layer. On a full back surface side thereof, an electrode composed of metal such as aluminum is formed. Moreover, a scintillator is fixed to each groove in an insertion manner.

DISCLOSURE OF THE INVENTION

[0003] However, since the electrode is provided on an incident surface side (surface side of the silicon wafer) of scintillation light (radiation) in the semiconductor energy detector constituted as described above, it becomes impossible to detect the scintillation light in a portion where the electrode is provided. Thus, there have been limitations on enlarging an area of a portion where it becomes possible to detect the scintillation light in the semiconductor energy detector.

[0004] The present invention was created in consideration of the above-described point. An object of the present invention is to provide a semiconductor energy detector capable of enlarging the area of the portion where it becomes possible to detect the energy ray.

[0005] In order to attain the foregoing object, a semiconductor energy detector of the present invention includes: a semiconductor substrate comprised of a semiconductor of a first conductivity type, onto which an energy ray of a predetermined wavelength range is incident from an incident surface thereof, characterized in that a diffusion layer of a second conductivity type, the diffusion layer being comprised of a semiconductor of the second conductivity type, and a diffusion layer of a first conductivity type, the diffusion layer being comprised of a semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate, are provided on a surface opposite to the incident surface of the semiconductor substrate.

[0006] Since the diffusion layer of the second conductivity type and the diffusion layer of the first conductivity type are provided on the surface opposite to the incident surface of the semiconductor substrate, no electrode is provided on the incident surface of the semiconductor substrate, thus making it possible to enlarge the area of the portion where it becomes possible to detect the energy ray.

[0007] The semiconductor energy detector of the present invention may be characterized in that a scintillator is optically connected to the incident surface of the semiconductor substrate.

[0008] Since the scintillator is optically connected to the incident surface of the semiconductor substrate, the area of the portion where it becomes possible to detect the scintillation light can be enlarged.

[0009] The semiconductor energy detector of the present invention may be characterized in that, in the semiconductor substrate, a region that is not depleted from the surface opposite to the incident surface of the semiconductor substrate to the incident surface is provided in a completely depleted state where depletion is performed from the surface opposite to the incident surface of the semiconductor substrate to the incident surface.

[0010] In the semiconductor substrate, the region that is not depleted from the surface opposite to the incident surface of the semiconductor substrate to the incident surface is provided in the completely depleted state where the depletion is performed from the surface opposite to the incident surface of the semiconductor substrate to the incident surface. Thus, when a bias voltage is being applied through the diffusion layer of the first conductivity type, the adjacent depletion layers are connected below the diffusion layer of the first conductivity type, and the bias voltage cannot be applied to the diffusion layer of the first conductivity type any more. However, in the semiconductor substrate, the region that is not depleted from the surface opposite to the incident surface of the semiconductor substrate to the incident surface is provided in the completely depleted state where the depletion is performed from the surface opposite to the incident surface of the semiconductor substrate to the incident surface. Thus, even after the adjacent depletion layers are connected below the diffusion layer of the first conductivity type, the bias voltage can be continuously applied through the region that is not depleted from the surface opposite to the incident surface of the semiconductor substrate to the incident surface, thus making it possible to further deplete the semiconductor substrate. As a result of this, it becomes possible to restrict the lowering of a detection sensitivity and a response rate for the energy ray.

[0011] The semiconductor energy detector of the present invention may be characterized in that the diffusion layer of the first conductivity type includes: a first diffusion layer of the first conductivity type for separating the diffusion layers of the second conductivity type, the first diffusion layer of the first conductivity type being

provided between the diffusion layers of the second conductivity type; and a second diffusion layer of the first conductivity type formed to be wider than the first diffusion layer of the first conductivity type, the second diffusion layer of the first conductivity type being provided on the outside of an array of the diffusion layers of the second conductivity type.

[0012] The diffusion layer of the first conductivity type includes: the first diffusion layer of the first conductivity type for separating the diffusion layers of the second conductivity type, the diffusion layer of the first conductivity type being provided between the diffusion layers of the second conductivity type; and the second diffusion layer of the first conductivity type formed to be wider than the first diffusion layer of the first conductivity type, the second diffusion layer of the first conductivity type being provided on the outside of the array of the diffusion layers of the second conductivity type. Thus, a constitution capable of providing the region that is not depleted from the surface opposite to the incident surface of the semiconductor substrate to the incident surface in the completely depleted state where the depletion is performed from the surface opposite to the incident surface of the semiconductor substrate to the incident surface can be realized in the semiconductor substrate simply at low cost.

[0013] Moreover, the semiconductor energy detector of the present invention may be characterized in that a sum of a width of the diffusion layer of the second conductivity type adjacent to the second diffusion layer of the first conductivity type and a width of the second diffusion layer of the first conductivity type is set equal to a sum of a width of the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type and a width of the first diffusion layer of the first conductivity type.

[0014] The sum of the width of the diffusion layer of the second conductivity type that is adjacent to the second diffusion layer of the first conductivity type and the width of the second diffusion layer of the first conductivity type is set equal to the sum of the width of the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type and the width of the first diffusion layer of the first conductivity type. Thus, a width of a unit region including the diffusion layer of the second conductivity type adjacent to the second diffusion layer of the first conductivity type becomes equal to a width of a unit region including the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type. Thus, particularly in the case of arraying a plurality of the semiconductor substrates, each having the diffusion layer of the second conductivity type and the diffusion layer of the first conductivity type provided therein, widths of all the unit regions become equal, thus making it possible to further enlarge the area of the portion where it becomes possible to detect the energy ray.

[0015] Moreover, the semiconductor energy detector of the present invention may be characterized in that the second diffusion layer of the first conductivity type is provided on a periphery of the semiconductor substrate.

[0016] The second diffusion layer of the first conductivity type is provided on the periphery of the semiconductor substrate. Thus, on the periphery of the semiconductor substrate, the undepleted region exists below the second diffusion layer of the first conductivity type, and thus it is possible to restrict the increase of a leakage current generated by a connection of the depletion layer to the periphery of the semiconductor substrate.

[0017] Moreover, the semiconductor energy detector of the present invention may be characterized in that a plurality of the diffusion layers of the second conductivity type are arrayed at a predetermined interval, the first diffusion layers of the first conductivity type for separating the diffusion layer of the second conductivity type is provided between the diffusion layers of the second conductivity type, the first diffusion layers being comprised of the semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate, and the second diffusion layer of the first conductivity type is provided on an outside of an array of the diffusion layers of the second conductivity type, the second diffusion layer being formed to be wider than the first diffusion layer of the first conductivity type and being comprised of the semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate.

[0018] The diffusion layers of the second conductivity type, the first diffusion layer of the first conductivity type and the second diffusion layer of the first conductivity type are provided on the surface side opposite to the incident surface of the semiconductor substrate. Therefore, no insensitive region caused by extracting an electrode is formed on the incident surface side of the energy ray, thus making it possible to enlarge the area of the portion where it becomes possible to detect the energy ray.

[0019] When the bias voltage is being applied through the first diffusion layer of the first conductivity type, the depletion layers adjacent to each other are connected below the first diffusion layer of the first conductivity type, and the bias voltage cannot be applied to the first diffusion layer of the first conductivity type any more. However, on the outside of the array of the diffusion layers of the second conductivity type, the second diffusion layer of the first conductivity type is provided, which is formed to be wider than the first diffusion layer of the first conductivity type and comprised of the semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate. Therefore, even after the adjacent depletion layers are connected to each other below the first diffusion layer of the first conductivity type, the bias voltage can be continuously applied through the second diffusion layer of the first conductivity type, thus making it possible to further ad-

vance the depletion of the semiconductor substrate. As a result of this, in the semiconductor energy detector, it becomes possible to restrict the lowering of a detection sensitivity and a response rate for the energy ray.

[0020] Moreover, the semiconductor energy detector of the present invention may be characterized in that the sum of a width of the diffusion layer of the second conductivity type adjacent to the second diffusion layer of the first conductivity type and the width of the second diffusion layer of the first conductivity type is set equal to the sum of the width of the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type and the width of the first diffusion layer of the first conductivity type.

[0021] The sum of the width of the diffusion layer of the second conductivity type adjacent to the second diffusion layer of the first conductivity type and the width of the second diffusion layer of the first conductivity type is set equal to the sum of the width of the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type and the width of the first diffusion layer of the first conductivity type. Thus, a width of a unit region including the diffusion layer of the second conductivity type adjacent to the second diffusion layer of the first conductivity type becomes equal to a width of a unit region including the diffusion layer of the second conductivity type that is not adjacent to the second diffusion layer of the first conductivity type. Thus, particularly in the case of arraying a plurality of the semiconductor energy detectors of the present invention, the widths of all the unit regions become equal, thus making it possible to further enlarge the area of the portion where it becomes possible to detect the energy ray.

[0022] Moreover, the semiconductor energy detector of the present invention may be characterized in that the second diffusion layer of the first conductivity type is provided on a periphery of the semiconductor substrate.

[0023] The second diffusion layer of the first conductivity type is provided on the periphery of the semiconductor substrate. Thus, on the periphery of the semiconductor substrate, the undepleted region exists below the second diffusion layer of the first conductivity type, and thus it is possible to restrict the increase of a leakage current generated by a reach of the depletion layer to the periphery of the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024]

Fig. 1 is a perspective view showing an energy ray detector.

Fig. 2 is a plan view showing a back-surface-incident-type photodiode array included in the energy ray detector.

Fig. 3 is a schematic view showing a cross-sectional structure of the back-surface-incident-type photodiode array included in the energy ray detector.

Fig. 4 is a schematic view showing a cross-sectional structure of the back-surface-incident-type photodiode array included in the energy ray detector.

Fig. 5 is a schematic view showing a cross-sectional structure of the back-surface-incident-type photodiode array included in the energy ray detector.

Fig. 6 is a plan view showing a state where the back-surface-incident-type photodiode arrays, each being included in the energy ray detector, are arrayed in the form of matrix.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025] Description will be made for an energy ray detector according to an embodiment of the present invention with reference to the drawings. Note that, in the respective drawings, the same reference numerals will be used for the same elements or elements having the same functions, and repeated description will be omitted.

[0026] As shown in Fig. 1, an energy ray detector R includes a photodiode array 1 and a scintillator 2, and functions as a radiation detector. The scintillator 2 is optically connected to one surface (incident surface) side of the photodiode array 1, and is constituted such that scintillation light occurring when radiation is incident onto the scintillator 2 is made incident onto the photodiode array 1. Note that, on the surface of the scintillator 2, onto which the radiation is incident, Al, Cr or the like may be evaporated to form a reflection film that transmits the incident radiation therethrough and reflects the scintillation light from the scintillator 2.

[0027] Next, description will be made for a constitution of the photodiode array 1 with reference to Fig. 2 and Fig. 3. In this embodiment, as the photodiode array 1, a back-surface-incident-type photodiode array of a complete depletion type, of which number of photodiodes is 25 (5×5), is used.

[0028] As shown in Fig. 2 and Fig. 3, the back-surface-incident-type photodiode array 1 includes a semiconductor substrate 3, and on this semiconductor substrate 3, the photodiode array is formed. The semiconductor substrate 3 is composed of a high-resistance N-type silicon substrate having a wafer thickness of 0.3 mm and a specific resistance of 5 kΩ·cm.

[0029] The photodiode array 1 includes P^+ diffusion layers 4 and 5 as diffusion layers of a second conductivity type, an N^+ channel stop layer 6 as a first diffusion layer of a first conductivity type, an N^+ channel stop layer 7 as a second diffusion layer of the first conductivity type, an N^+ diffusion layer 8, wiring 9 composed of aluminum or the like, and an AR (anti-reflective) coating layer 10. The P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7 are provided on a surface side opposite to the incident surface of the semiconductor substrate 3, onto which the scintillation light is incident from the scintillator 2. The N^+ diffusion layer 8 is

provided on an incident surface side of the semiconductor substrate 3, onto which the scintillation light is incident from the scintillator 2. On the N^+ diffusion layer 8, the AR (anti-reflective) coating layer 10 is provided. The N^+ diffusion layer 8 is composed of a semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate 3, and a surface concentration thereof is set at approximately 1.0×10^{19} cm^{-3}. The scintillator 2 is optically connected to the surface (incident surface) opposite to the surface of the semiconductor substrate 3, on which the P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7 are provided.

[0030] The P^+ diffusion layers 4 and 5 have surface concentrations set at approximately 1.0×10^{20} cm^{-3}, and 5×5 (25) elements thereof are arrayed at a predetermined interval (in this embodiment, approximately 500 μm) spaced therebetween.

[0031] The N^+ channel stop layer 6 is composed of the semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate 3, and a surface concentration of the N^+ channel stop layer 6 is set at approximately 1.0×10^{19} cm^{-3}. Moreover, the N^+ channel stop layer 6 is provided between the P^+ diffusion layers 4, 5 adjacent to each other, and exhibits a lattice shape so as to separate the P^+ diffusion layers 4, 5. Intervals between the P^+ diffusion layer 4, 5 and the N^+ channel stop layer 6 are set at approximately 150 μm. A width of the N^+ channel stop layer 6 is set at approximately 200 μm.

[0032] The N^+ channel stop layer 7 is composed of the semiconductor of the first conductivity type higher in impurity concentration than the semiconductor substrate 3, and a surface concentration of the N^+ channel stop layer 7 is set at approximately 1.0×10^{19} cm^{-3}. Moreover, the N^+ channel stop layer 7 is provided in the form of frame on the outside of the array of the P^+ diffusion layers 4 and 5 continuously with the N^+ channel stop layer 6. An interval between the N^+ diffusion layer 5 and the N^+ channel stop layer 7 is set at approximately 300 μm, and a distance from the N^+ diffusion layer 5 including the N^+ channel stop layer 7 to a periphery of the semiconductor substrate 3 is approximately 900 μm. A width of the N^+ channel stop layer 7 is set at approximately 600 μm, and the N^+ channel stop layer 7 is set wider than the N^+ channel stop layer 6.

[0033] The P^+ diffusion layer 5 that is adjacent to the N^+ channel stop layer 7 is set shorter in width as compared with the P^+ diffusion layer 4 that is not adjacent to the N^+ channel stop layer 7. The sum of the width of the P^+ diffusion layer 5 that is adjacent to the N^+ channel stop layer 7 and the width of the N^+ channel stop layer 7 is set equal to the sum of the width of the P^+ diffusion layer 4 that is not adjacent to the N^+ channel stop layer 7 and the width of the N^+ channel stop layer 6. Thus, though an area of the P^+ diffusion layer 5 becomes smaller than an area of the P^+ diffusion layer 4, a width of a photodiode unit cell (unit region) including the P^+ diffusion layer 5 becomes equal to the width of the photodiode unit cell (unit region) including the P^+ diffusion layer 4. Therefore, the areas of the photodiode unit cells (unit regions) of the photodiode array 1 become all equal.

[0034] On the wiring 9 electrically connected to each of the P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7, a bump 11 is formed. Electrical connections of the P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7 are made on the surface side opposite to the incident surface of the semiconductor substrate 3. The bump 11 is connected to an output readout circuit (not shown) by flip chip bonding.

[0035] Next, description will be made for an operation of the photodiode array 1 constituted as described above with reference to Fig. 4 and Fig. 5.

[0036] First, in the case of using the photodiode array 1 by applying a positive bias voltage to the N^+ channel stop layers 6 and 7, depletion layers 12 in accordance with a size of the bias voltage are formed in the semiconductor substrate 3. In the photodiode array 1, when the bias voltage is being applied through the N^+ channel stop layers 6 and 7, as shown in Fig. 4, the depletion layers 12 adjacent to each other are connected below the N^+ channel stop layer 6 in a state where a voltage of approximately 100 V on the way of complete depletion is applied thereto. Thus, a state is brought, where a bias voltage more than or equal to the approximately 100 V described above cannot be applied to the N^+ channel stop layer 6. Note that, in a PIN-type photodiode using a high-resistance N-type silicon substrate having a specific resistance of 5 kΩ·cm, which is the same as the semiconductor substrate 3, usually, the complete depletion is achieved by applying a bias voltage of approximately 110 V to 120 V.

[0037] However, the N^+ channel stop layer 7 wider than the N^+ channel stop layer 6 is provided on the outside of the array of the P^+ diffusion layers 4 and 5 continuously with the N^+ channel stop layer 6. Therefore, from below the N^+ channel stop layer 7 to the incident surface side of the semiconductor substrate 3, a region 13 where the depletion layer 12 is not formed exists as a region that is not depleted. Hence, since the region 13 where the depletion layer 12 is not formed is provided from below the N^+ channel stop layer 7 to the incident surface side of the semiconductor substrate 3, the bias voltage can be applied to the N^+ diffusion layer 8 through the N^+ channel stop layer 7 even after the adjacent depletion layers 12 are connected below the N^+ channel stop layer 6. Therefore, the depletion in the semiconductor substrate 3 can be further advanced.

[0038] The bias voltage is further applied continuously even after the depletion layers 12 reach the N^+ diffusion layer 8, and thus it is possible to reduce or eliminate the insensitive region (depletion layer 12) below the N^+ channel stop layer 6. By applying a bias voltage of approximately 200 V, as shown in Fig. 5, the depletion layer 12 is expanded over the full incident surface (N^+ dif-

fusion layer 8) of the semiconductor substrate 3, and the semiconductor substrate 3 is put in a state of being completely depleted. Even in the state where the semiconductor substrate 3 is completely depleted, as shown in Fig. 5, the region 13 where the depletion layer 12 is not formed is provided from below the N^+ channel stop layer 7 to the incident surface side of the semiconductor substrate 3.

[0039] In the state where the depletion layer 12 reaches the N^+ diffusion layer 8 of the semiconductor substrate 3, when the scintillation light is incident from the scintillator 2 onto the incident surface of the semiconductor substrate 3, a photoelectric current generated in the depletion layer 12 is detected at a high speed in the photodiode array 1. Moreover, since the photodiode unit cells including the P^+ diffusion layers 4 and 5 are arranged in the form of matrix (multi-channelized), an incident position of the scintillation light is also detected in the photodiode array 1.

[0040] When the depletion layer 12 reaches to the periphery of the semiconductor substrate 3, a leakage current is increased. However, since the N^+ channel stop layer 7 is set wider than the N^+ channel stop layer 6, the region 13 where the depletion layer 12 is not formed exists below the N^+ channel stop layer 7. Thus, it is possible to restrict the increase of the leakage current in the periphery of the semiconductor substrate 3.

[0041] As described above, the energy ray detector R includes the photodiode array 1 and the scintillator 2. On the surface side opposite to the incident surface of the semiconductor substrate 3 in the photodiode array 1, the P^+ diffusion layers 4 and 5 and the N^+ channel stop layers 6 and 7 are provided, and the scintillator 2 is optically connected to the incident surface side of the semiconductor substrate 3. As described above, since no electrode is provided on the incident surface side of the semiconductor substrate 3, no insensitive region caused by extracting an electrode is formed, thus making it possible to enlarge an area of a portion where it becomes possible to detect radiation.

[0042] Moreover, since no electrode is provided on the incident surface side of the semiconductor substrate 3, the incident surface side of the semiconductor substrate 3 can be planarized, thus facilitating the scintillator 2 to be optically connected thereto.

[0043] When the bias voltage is being applied through the N^+ channel stop layer 6, the adjacent depletion layers 12 are connected to each other below the N^+ channel stop layer 6, and the bias voltage cannot be applied to the N^+ channel stop layer 6 any more. However, since the N^+ channel stop layer 7 is provided on the semiconductor substrate 3 of the photodiode array 1, the region 13 where the depletion layer 12 is not formed is provided from below the N^+ channel stop layer 7 to the incident surface side of the semiconductor substrate 3. Thus, even after the adjacent depletion layers 12 are connected to each other below the N^+ channel stop layer 6, the bias voltage can be continuously applied through the N^+ channel stop layer 7, and the depletion of the semiconductor substrate 3 can be further advanced, thus making it possible to completely deplete the semiconductor substrate 3. As a result of this, in the photodiode array 1, it becomes possible to restrict the lowering of a detection sensitivity and a response rate for the energy ray.

[0044] Moreover, the N^+ channel stop layer 7 set wider than the N^+ channel stop layer 6 is provided on the outside of the array of the P^+ diffusion layers 4 and 5, thus making it possible to provide the region 13 where the depletion layer 12 is not formed in the portion of the semiconductor substrate 3 from the surface provided with the N^+ channel stop layers 6 and 7 to the incident surface. As a result of this, a constitution capable of providing the region 13 where the depletion layer 12 is not formed can be realized simply at low cost.

[0045] Note that the photodiode array 1 is basically used in a completely depleted state where the depletion layers 12 are expanded over the full incident surface (N^+ diffusion layer 8). In this completely depleted state, the depletion layers 12 are all connected below the N^+ channel stop layer 6, and the depletion layers 12 reach the vicinities of the peripheries of the semiconductor substrate 3. Since this expansion of the depletion layers 12 to the vicinities of the peripheries of the semiconductor substrate 3 can be adjusted by the applied bias voltage, even if the P^+ diffusion layer 5 is made small, it is possible to expand the depletion layer 12 to the vicinities of the peripheries of the semiconductor substrate 3. Thus, even in the case of setting the width (area) of the P^+ diffusion layer 5 smaller than the width (area) of the P^+ diffusion layer 4, carriers generated in the depletion layer 12 are collected to the P^+ diffusion layer 5. As a result of this, a reduction of the sensitive region of the photodiode array 1 is restricted, and a light sensitivity of the photodiode array 1 for the scintillation light is restricted from being affected.

[0046] Moreover, as shown in Fig. 6, the photodiode array 1 can be used such that a plurality of the photodiode arrays 1 are arrayed in the form of matrix.

[0047] The sum of the width of the P^+ diffusion layer 5 that is adjacent to the N^+ channel stop layer 7 and the width of the N^+ channel stop layer 7 is set so as to be equal to the sum of the width of the P^+ diffusion layer 4 that is not adjacent to the N^+ channel stop layer 7 and the width of the N^+ channel stop layer 6. Thus, as shown in Fig. 6, the width "a" of the photodiode unit cell (unit region) including the P^+ diffusion layer 5 becomes equal to the width "a" of the photodiode unit cell (unit region) including the P^+ diffusion layer 4. Thus, the areas of the photodiode unit cells (unit regions) in the photodiode array 1 become all equal. As a result of this, in the case of arranging the plurality of photodiode arrays 1 in the form of matrix, the energy ray can be readily detected by a large area, and the incident position of the energy ray can be suitably detected.

[0048] Note that the N^+ channel stop layer 7 does not have to be provided on the periphery of the semicon-

ductor substrate 3, and may be provided on a position of any of the N^+ channel stop layers 6 (position between the photodiode unit cells). However, since the region 13 below the N^+ channel stop layer 7 is not depleted, an insensitive region exists between the photodiode unit cells of the photodiode array 1. Hence, in order to avoid two phenomena: an insensitive region exists between the photodiode unit cells of the photodiode array 1; and a leakage current is generated in the periphery of the semiconductor substrate 3, preferably, the N^+ channel stop layer 7 is provided on the periphery of the semiconductor substrate 3.

[0049] The present invention is not limited to the above-described embodiment, and the foregoing numerical values and the like can be appropriately changed and set. Moreover, the present invention can be applied to a variety of semiconductor energy detectors other than the radiation detector.

INDUSTRIAL APPLICABILITY

[0050] The present invention can be utilized for the semiconductor energy detector such as the radiation detector.

Claims

1. A semiconductor energy detector, comprising:

    a semiconductor substrate comprised of a semiconductor of a first conductivity type, onto which an energy ray of a predetermined wavelength range is incident from an incident surface thereof,

    wherein a diffusion layer of a second conductivity type comprised of a semiconductor of a second conductivity type and a diffusion layer of the first conductivity type comprised of a semiconductor of the first conductivity type higher in impurity concentration than said semiconductor substrate are provided on a surface opposite to the incident surface of said semiconductor substrate.

2. The semiconductor energy detector according to claim 1,
    wherein a scintillator is optically connected to the incident surface of said semiconductor substrate.

3. The semiconductor energy detector according to claim 1,
    wherein, in said semiconductor substrate, a region not being depleted from the surface opposite to the incident surface of said semiconductor substrate to the incident surface is provided in a completely depleted state where depletion is performed from the surface opposite to the incident surface of said semiconductor substrate to the incident surface.

4. The semiconductor energy detector according to claim 3,
    wherein said diffusion layer of the first conductivity type includes:

    a first diffusion layer of the first conductivity type for separating said diffusion layers of the second conductivity type, said first diffusion layer of the first conductivity type being provided between said diffusion layers of the second conductivity type; and
    a second diffusion layer of the first conductivity type formed to be wider than said first diffusion layer of the first conductivity type, said second diffusion layer of the first conductivity type being provided on the outside of an array of said diffusion layers of the second conductivity type.

5. The semiconductor energy detector according to claim 4,
    wherein a sum of a width of said diffusion layer of the second conductivity type adjacent to said second diffusion layer of the first conductivity type and a width of said second diffusion layer of the first conductivity type is set equal to a sum of a width of said diffusion layer of the second conductivity type not being adjacent to said second diffusion layer of the first conductivity type and a width of said first diffusion layer of the first conductivity type.

6. The semiconductor energy detector according to claim 4,
    wherein said second diffusion layer of the first conductivity type is provided on a periphery of said semiconductor substrate.

7. The semiconductor energy detector according to claim 1,
    wherein a plurality of said diffusion layers of the second conductivity type are arrayed at a predetermined interval,
    a first diffusion layer of the first conductivity type for separating said diffusion layers of the second conductivity type is provided between said diffusion layers of the second conductivity type, said first diffusion layer of the first conductivity type being comprised of the semiconductor of the first conductivity type higher in impurity concentration than said semiconductor substrate, and
    on an outside of an array of said diffusion layers of the second conductivity type, a second diffusion layer of the first conductivity type is provided, said second diffusion layer of the first conductivity type being formed to be wider than said first diffu-

sion layer of the first conductivity type and being comprised of the semiconductor of the first conductivity type higher in impurity concentration than said semiconductor substrate.

8. The semiconductor energy detector according to claim 7,
wherein a sum of a width of said diffusion layer of the second conductivity type adjacent to said second diffusion layer of the first conductivity type and a width of said second diffusion layer of the first conductivity type is set equal to a sum of a width of said diffusion layer of the second conductivity type not being adjacent to said second diffusion layer of the first conductivity type and a width of said first diffusion layer of the first conductivity type.

9. The semiconductor energy detector according to claim 7,
wherein said second diffusion layer of the first conductivity type is provided on a periphery of said semiconductor substrate.

Fig.1

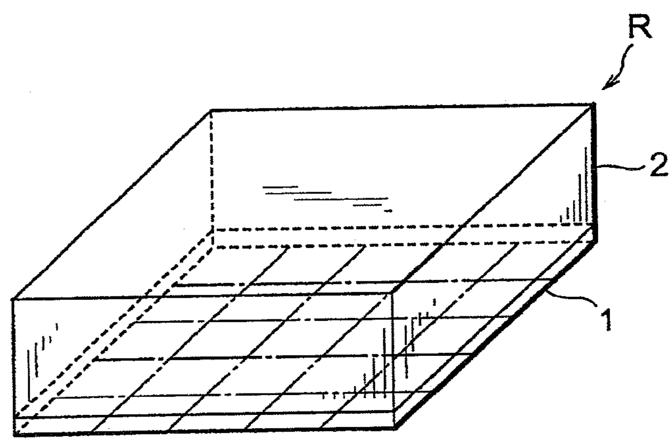
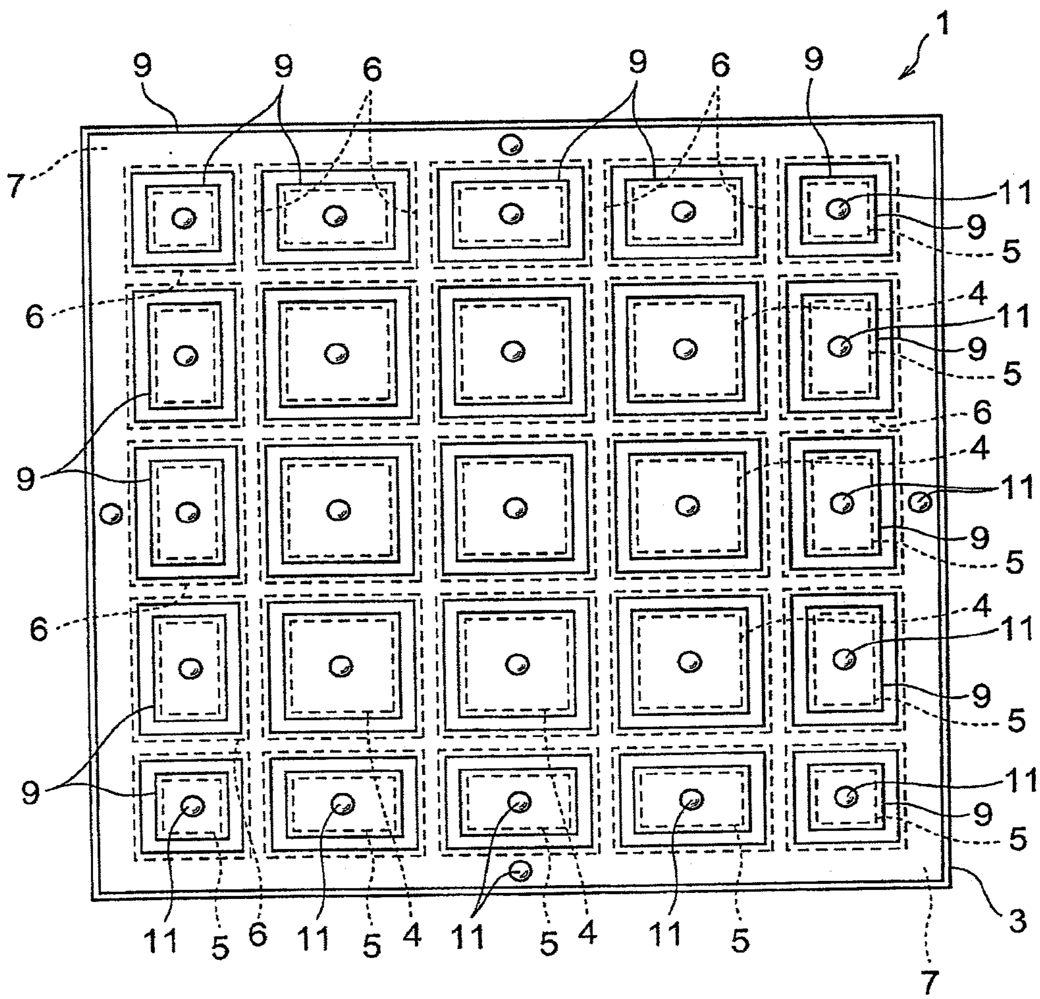


Fig.2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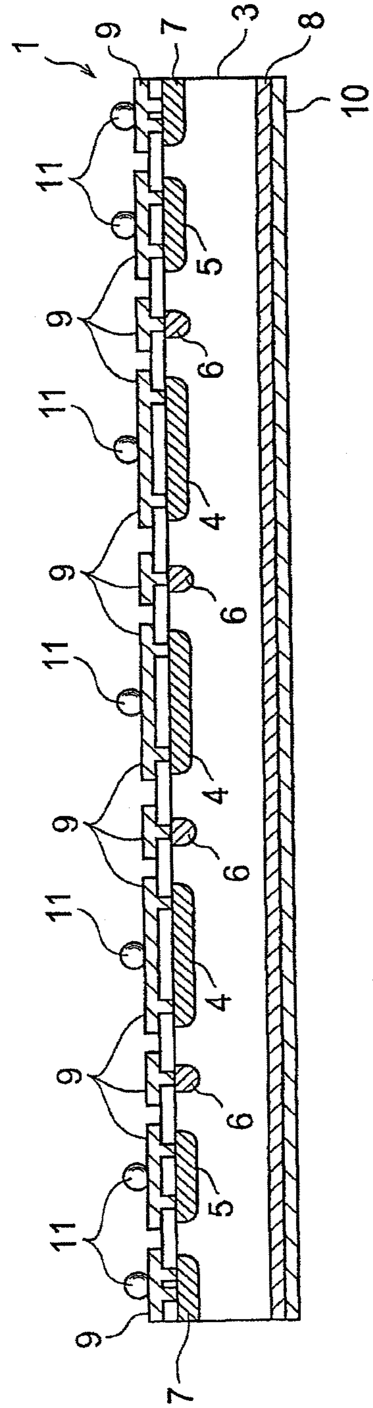


Fig.3

Fig.4

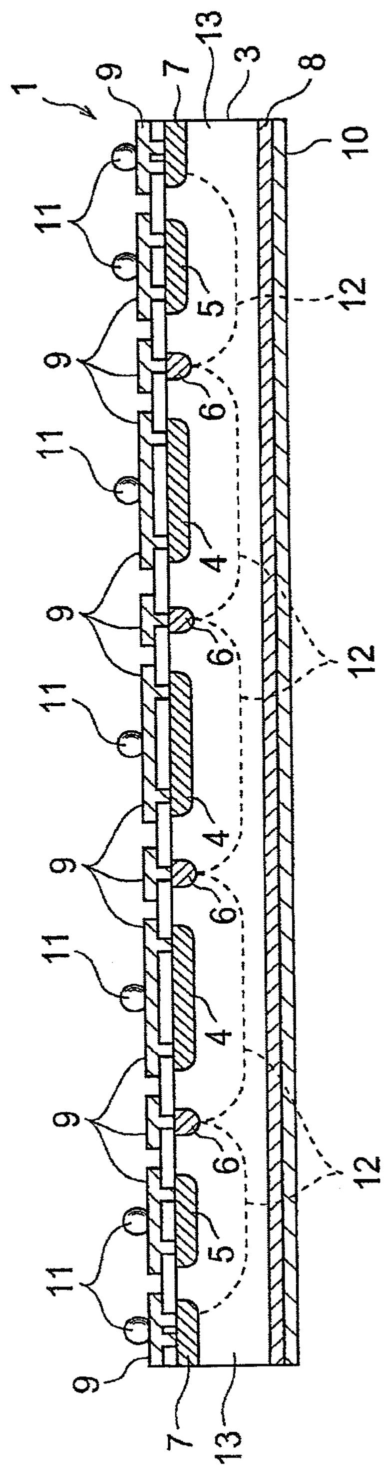


Fig.5

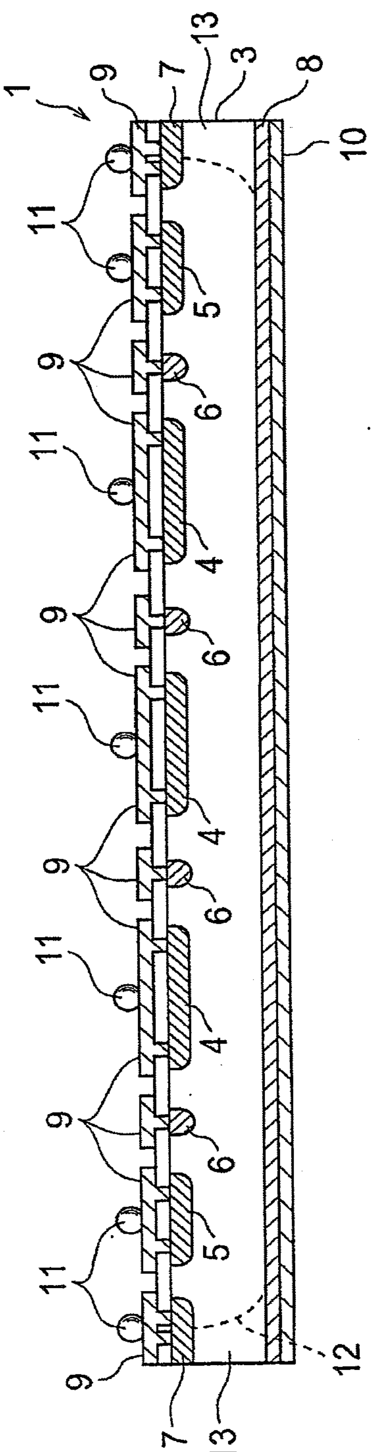
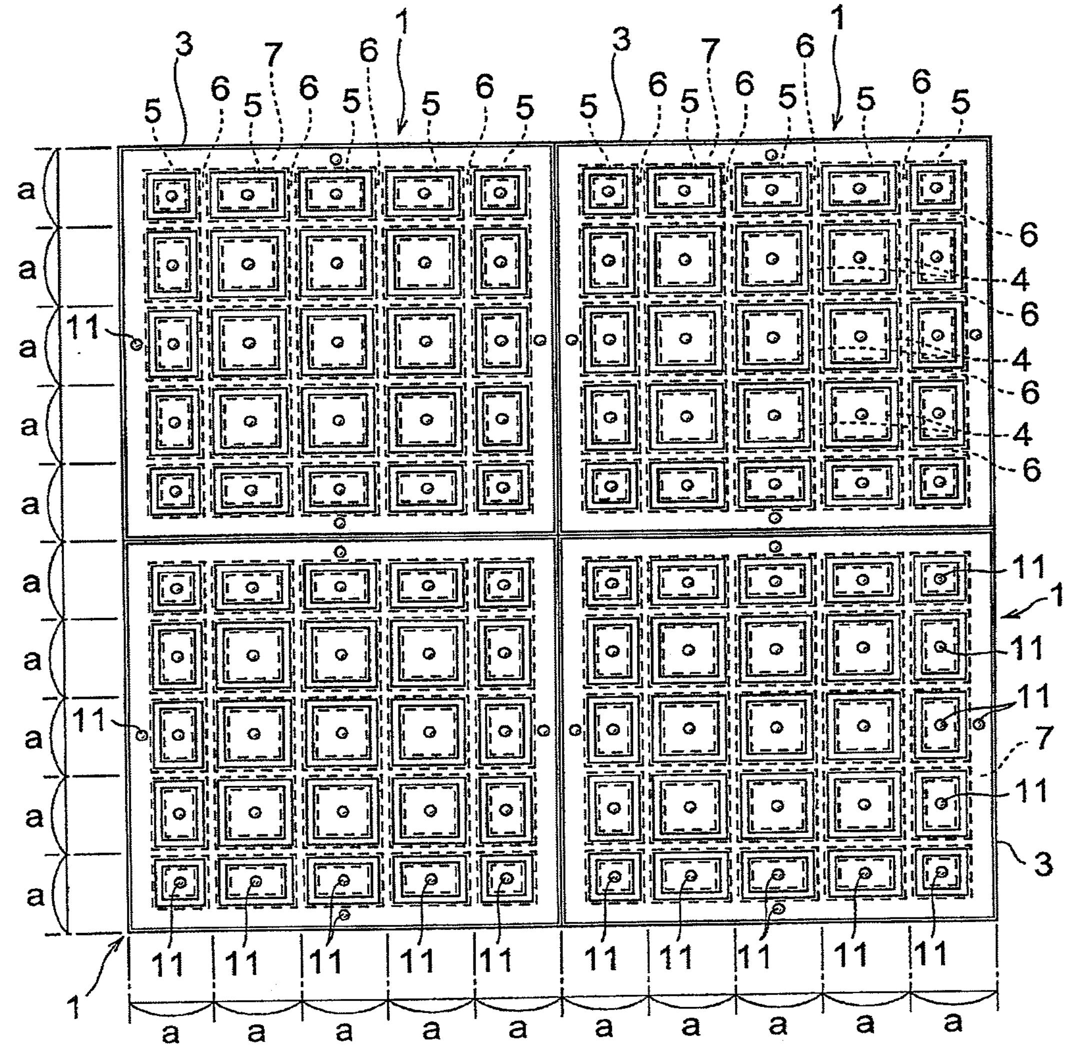


Fig.6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/02568

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl⁷ H01L27/142, H04N5/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl⁷ H01L27/14-148

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Toroku Jitsuyo Shinan Koho	1994-2001
Kokai Jitsuyo Shinan Koho	1971-2001	Jitsuyo Shinan Toroku Koho	1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 10-209417, A (SII RD Center K.K.), 07 August, 1998 (07.08.98), Full text; Fig. 3 & US, 6114685, A	1-2
X	JP, 6-140613, A (Hamamatsu Photonics K.K.), 20 May, 1994 (20.05.94), Full text; Fig. 3 (Family: none)	1
X	JP, 3-148869, A (Fujitsu Limited), 25 June, 1991 (25.06.91), Full text; Fig. 8 (Family: none)	1
A	US, 5777352, A (Eastman Kodak Company), 07 July, 1998 (07.07.98), Full text; Fig. 5 (Family: none)	1

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search 22 June, 2001 (22.06.01)	Date of mailing of the international search report 03 July, 2001 (03.07.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/02568

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 9-331051, A (SII RD Center K.K.), 22 December, 1997 (22.12.97), Full text; Fig. 1 (Family: none)	1

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